REMARKS

Claims 1-39 are pending in the application.

Claims 1, 2, 24-29 and 33-36 have been rejected.

Claims 3, 30-32 and 37-39 have been objected to.

Claims1-39 remain pending in this application.

Reconsideration of the claims is respectfully requested.

I. ALLOWABLE SUBJECT MATTER

The Examiner stated that Claims 3, 30-32 and 37-39 are objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim. (August 5, 2008 Office Action, Page 4, Paragraph 7). The Applicants thank the Examiner for the indication that Claims 3, 30-32 and Claims 37-39 would be allowable if rewritten in independent form to incorporate the elements of their respective base claims and any intervening claims. Because the Applicants believe that the remaining claims in this application are allowable, the Applicants have not rewritten Claim 3, Claims 30-32 and Claims 37-39 in independent form at this time.

II. CLAIM REJECTIONS -- 35 U.S.C. § 102

Claims 1-2, 24-29 and 33-36 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,469,585 to Dai et al. (hereinafter "*Dai*"). The Applicants respectfully traverse these rejections for the reasons set forth below.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

The Examiner stated that the circuit shown in Figure 3 of the *Dai* reference anticipates the Applicants' invention as claimed in Claims 1-2, 24-29 and 33-36. (August 5, 2008 Office Action, Pages 2-3). The Applicants respectfully point out that the circuit that is shown in Figure 3 of the *Dai* reference is a delay stage 32 for a ring-type voltage controlled oscillator 30. The delay stage 32 comprises inverters (33 and 34), a memory circuit (35) and tuning circuitry (transistors M1, M4, M7 and M10). The transistors of the tuning circuitry function as variable resistors to tune the amount of delay of the delay stage 32, and hence the frequency of the voltage controlled oscillator 30. (*Dai*, Column 4, Lines 23-28). The frequency (not the phase) is tuned. Therefore, the *Dai* reference does not show a phase shifter circuit.

The *Dai* reference states that each delay stage (32A and 32B) causes a ninety degree phase shift. The *Dai* reference states "Each delay stage 32A and 32B causes a 90° phase shift, and so the phase shifts relative to V_{OUT+} of delay stage 32A are as follows – V_{OUT+} of delay stage 32A is shifted 90°, V_{OUT-} of delay stage 32A is shifted 180°, and V_{OUT-} of delay stage 32B is shift[ed] 270°." (*Dai*, Column 3, Lines 54-59).

It is clear that the *Dai* delay stages (32A and 32B) each cause a fixed phase shift of 90°. The value of phase shift is 90° is a fixed value and is not a variable value. Therefore, the delay stages (32A and 32B) of the *Dai* reference are not "variable phase shifting circuits." Because the claims of the Applicants' patent application require a variable phase shifting circuit (and not a fixed phase shifting circuit), the *Dai* reference does not anticipate the Applicants' invention.

The Examiner stated that the transistors M1 and M7 and the cross coupled transistors M5 and M6 in the *Dai* reference form a synchronized oscillator that maintain an oscillation of the output signal. (August 5, 2008 Office Action, Page 2, Lines 21-23). The Applicants respectfully traverse this assertion of the Examiner. The *Dai* reference states that "The memory element 35 in the configuration shown in FIG. 3 operates to prevent the outputs of inverters 33 and 34 from switching states when they otherwise would switch. In other words, memory element 35 causes switching to be delayed." (*Dai*, Column 5, Lines 58-62). The Applicants respectfully submit that the cross coupled transistors M5 and M6 operate as a memory element 35 and not as a synchronized oscillator.

The cross coupled transistors M5 and M6 constitute a very stable circuit 35 (as it must be for a memory, namely a latch). The electrical state of this memory circuit 35 can only be

changed by applying a switching signal at the input. In the absence of such switching signal input to the cross coupled transistors M5 and M6, there will be no variation at the output. Therefore, the memory circuit 35 can not be equivalent to an oscillator circuit.

Furthermore, the *Dai* reference states that "In accordance with the invention, the strength of inverters 33 and 34 is variable and dependent upon the control voltage received by the tuning transistors M1, M4, M7 and M10, whereas the strength of the memory element 35 remains relatively constant as it is tied, in the case of FIG. 3, to the power supply voltage V_{DD}. (*Dai*, Column 5, Line 67 to Column 6, Line 6) (Emphasis added). Because the strength of the memory element 35 remains relatively constant, the memory element 35 is not a synchronized oscillator that has a variable free-running oscillation frequency that is controlled by a control signal. There is no control signal in the *Dai* reference that controls the relatively constant memory element 35. This is because the cross coupled transistors M5 and M6 operate as a memory element 35 and not as a synchronized oscillator.

For these reasons, the elements of the *Dai* reference do not anticipate the Applicants' invention as claimed in Claims 1-2, 24-29 and 33-36. Accordingly, the Applicants respectfully request withdrawal of the §102 rejections and full allowance of Claims 1-2, 24-29 and 33-36.

III. CONCLUSION

For the foregoing reasons, the Applicants respectfully request full allowance of all pending claims (Claims 1-39) and that this application be passed to issuance.

The Applicants' attorney has made the amendments and arguments set forth above in order to place this application in condition for allowance. In the alternative, the Applicants' attorney has made the amendments and arguments to properly frame the issues for appeal. The Applicants make no admission concerning any now moot rejection or objection, and affirmatively denies any position, statement or averment of the Examiner that was not specifically addressed herein.

CONCLUSION

As a result of the foregoing, the Applicants assert that the remaining Claims in the Application are in condition for allowance, and respectfully request an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK CARTER, P.C.

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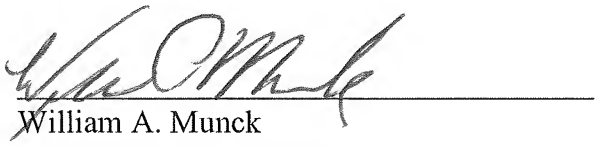

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